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14 and ((vertical near? control) or (control near? sidewall))

#	U	I	P	T	D	Document ID	Issue Date	Pages	Title	Current OR	Current NR	Retrieval	Inventor	E	C	R	A
39	F	F	F	N	B2	US 6809372	20041026	17	Flash memory structure using sidewall floating integrated circuit	257/315	257/316; 257/317		Gambino; Jeffrey P.; et al.	F	F	F	F
40	F	F	F	N	B2	US 6778441	20040817	33	memory device and method	365/185.25	257/315; 257/316;		Forbes; Leonard et al.	F	F	F	F
41	F	F	F	N	B2	US 6754108	20040622	26	DRAM cells with repressed floating gate	365/185.25	257/E29.12		Forbes; Leonard et al.	F	F	F	F
42	F	F	F	N	B1	US 6740927	20040525	12	Nonvolatile memory capable of storing mult	257/315	257/316; 257/321		Jeng; Erik S.	F	F	F	F
43	F	F	F	N	B2	US 6734067	20040511	32	Method of forming a semiconductor storage d	438/266	257/E21.68		Noro; Fumihiko et al.	F	F	F	F
44	F	F	F	N	B2	US 6727544	20040427	1730	Semiconductor memory including cell(s) with	257/315	257/296; 257/304;		Endoh; Tatsuo et al.	F	F	F	F
45	F	F	F	N	B2	US 6686532	20040203	20	Dual-bit multi-level thresholding NANDS memov	257/374	257/325; 257/E21.67		Ogura; Seiki et al.	F	F	F	F
46	F	F	F	N	B1	US 6630381	20031007	72	Preventing dielectric thickening over a float	438/260	257/E21.68		Hazani; Emanuel et al.	F	F	F	F
47	F	F	F	N	B2	US 6617636	20030909	63	Nonvolatile memory structures and fabricat	257/315	257/E21.62		Tuan; Hsing Ti et al.	F	F	F	F
48	F	F	F	N	B1	US 6586302	20030701	15	Method of using trenching techniques to	438/257	257/E21.20		Hopper; Peter J. et al.	F	F	F	F
49	F	F	F	N	B2	US 6528896	20030304	13	Scalable two transistor memory device	257/327	257/331; 257/304;		Song; Seunghoon et al.	F	F	F	F
50	F	F	F	N	B2	US 6512695	20030128	26	Field programmable	365/185.17	257/E21.20		Forbes; Leonard et al.	F	F	F	F